IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3 and 9-16 and ADD new claim 19 in accordance with the following:

1. (Currently Amended) An information processing unit, comprising:

a prefetch buffer ~~for fetching~~ prefetching an instruction through a bus with its width being ~~twice or more~~at least twice as large as an instruction length, to store the prefetched instruction;

a decoder ~~for~~ decoding the instruction stored in said prefetch buffer;

an arithmetic unit ~~for~~ executing the decoded instruction;

an instruction request control circuit performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch ~~the~~ instructions; and

a prefetch control circuit ~~fetching~~ prefetching the branch target instruction to said prefetch buffer when ~~the~~ a branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

2. (Original) The information processing unit according to claim 1, wherein said prefetch buffer prefetches the instruction from a main memory through an instruction cache memory.

3. (Currently Amended) The information processing unit according to claim 2, wherein said prefetch control circuit outputs to the instruction cache memory a control signal ~~for~~ canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent an access to the main memory, the access being caused by a cache miss.

4. (Original) The information processing unit according to claim 2, wherein said prefetch buffer prefetches the instruction from the instruction cache memory through a bus with

its width being twice as large as an instruction length, and outputs the instruction to said decoder through a bus with its width equal to the instruction length.

5. (Original) The information processing unit according to claim 4, wherein said prefetch buffer stores four pieces of instructions at maximum.

6. (Original) The information processing unit according to claim 1, wherein said decoder and said arithmetic unit perform operations in units of one instruction.

7. (Original) The information processing unit according to claim 1, wherein said instruction request control circuit and said prefetch control circuit perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

8. (Original) The information processing unit according to claim 1, wherein the branch instruction includes a conditional branch instruction and/or an unconditional branch instruction.

9. (Currently Amended) The information processing unit according to claim 1, further comprising a register ~~for~~ writing therein an execution result of said arithmetic unit.

10. (Currently Amended) An information processing method, comprising:

~~a first prefetch step of~~ prefetching an instruction through a bus with its width being ~~twice or more~~at least twice as large as an instruction length, to store the prefetched instruction;

~~a decode step of~~ decoding the prefetched instruction;

~~an execution step of~~ executing the decoded instruction;

~~an instruction request step of~~ performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch ~~the~~ instructions; and

~~a second prefetch step of~~ prefetching the branch target instruction when ~~the~~ a branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

11. (Currently Amended) The information processing method according to claim 10,

wherein said ~~first prefetch step~~prefetching an instruction prefetches the instruction from the main memory from ~~the~~ an instruction cache memory.

12. (Currently Amended) The information processing method according to claim 11, wherein said ~~second prefetch step~~ prefetching the branch target instruction outputs to the instruction cache memory a control signal ~~for~~ canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent the access to the main memory, the access being caused by a cache miss.

13. (Currently Amended) The information processing method according to claim 11, wherein said ~~first prefetch step~~prefetching an instruction prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length, and outputs the instruction to said ~~decode step~~decoding through a bus with its width equal to the instruction length.

14. (Currently Amended) The information processing method according to claim 13, wherein said ~~first prefetch step~~ prefetching an instruction stores 4 pieces of instructions at maximum.

15. (Currently Amended) The information processing method according to claim 10, wherein said ~~decode step~~ decoding and said ~~execution step~~executing perform operations in units of one instruction.

16. (Currently Amended) The information processing method according to claim 10, wherein said ~~instruction request step~~performing a prefetch request and said ~~second prefetch step~~prefetching the branch target instruction perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

17. (Original) The information processing method according to claim 10, wherein said branch instruction includes a conditional branch and/or an unconditional branch.

18. (Original) The information processing method according to claim 10, wherein said execution step writes an execution result to a register.

19. (New) An information processing method, comprising:

prefetching an instruction through a bus with a width at least twice as large as the length of the instruction, and storing the prefetched instruction;

performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch instructions; and

prefetching the branch target instruction when a branch is ensured to occur by executing the branch instruction, and ignoring the branch target instruction when a branch does not occur.